

Marketing Datasheet

ML4039-JIT-ATE

**4-Lane 8.5-15 & 21-30 Gbps/lane
Bit Error Rate Tester**

Stress Signal Generation

Vertical & Horizontal Eye Closure

Bathtub Curve Measurement

Eye Contour Measurement

Receiver Sensitivity

Jitter Tolerance

ML4039-JIT-ATE

4 Channel 30Gbps BERT



Summary

The **ML4039-JIT-ATE** series is a state-of-the-art, four-Lane Pulse Pattern Generator and Error Detector with Jitter Generator. It is fully equipped for laboratory and production testing of systems, components, and Electro-Optical modules.

Key Features

- Available in ATE form factors
- 8.5-15 and 21-30 Gbps data rate
- Low intrinsic jitter
- Automated J2/J9 measurement
- Integrated synthesizer
- Eye contour measurement
- Bathtub measurement
- Intuitive comprehensive GUI
- Window and Linux API functions
- Repeatable traceable measurement

RX Tolerance Measurement

- BER measurement
- Receiver mask tolerance

Ordering Information

ML4039-JIT-ATE: 4 Channels 30 Gbps BERT with Jitter Generation

Software Capabilities

- Provides LabVIEW drivers
- Multiple modules can be controlled via Fast Ethernet 100 BASE-TX

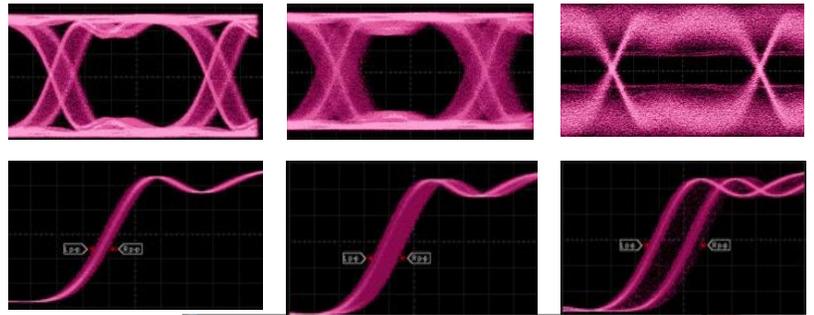
Target Applications

- Interconnect testing CFP2, CFP4, QSFP28
- Backplane testing
- Interference and crosstalk testing
- Receiver sensitivity testing
- Receiver jitter tolerance testing
- Electro-Optical module testing
- Electrical stressed eye testing for 100 Gbps Ethernet, MLD/CAUI application, OIF CEI-28GVSR, CPPI-4, CAUI-4, 32G Fiber Channel chip to module

ML4039-JIT

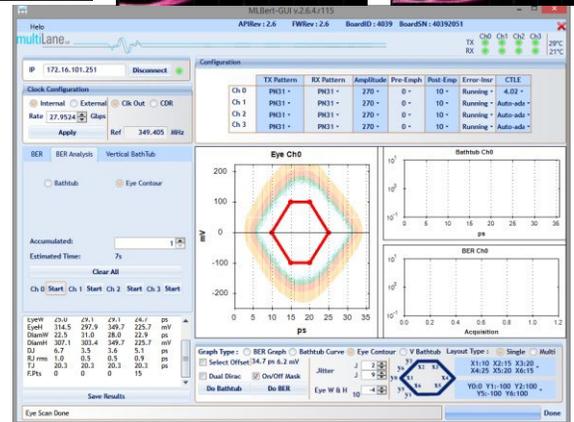
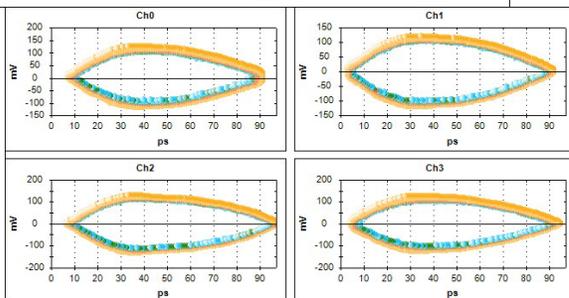
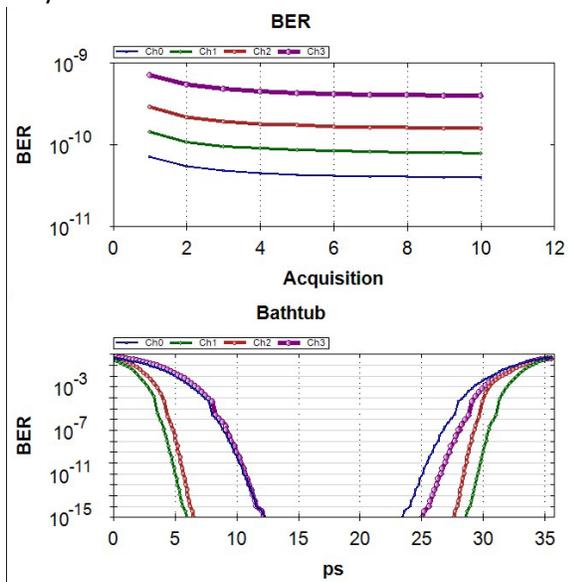
- Vertical and horizontal eye closure
- Vertical amplitude random noise injection
- Integrated, Calibrated Stress Generation to address the Stressed Receiver Sensitivity and Jitter Tolerance Test Requirements for a wide range of Standards.
 - Phase Shift
 - PM Sinusoidal Jitter
 - PM Random Jitter – AM Random Jitter

- Jitter tolerance compliance template testing with margin testing



ML BERT GUI

- Test 4-channel BER test at the same time
- Support BER curve
- Provide multiple and single layouts of bathtub and eye contour



Electrical Specification	
Bit Rate	8.5-15 & 21-30 Gbps
Data Format	NRZ
Pattern	PRBS 7, 9, 15, 23, 31, and User Defi Pattern 16 bits@10G & 40 bits@2
TX Amplitude Differential	100-2000 mV*
TX Amplitude Adjustment	5 mV/step
Pre-Emphasis	-
Pre-Emphasis Resolution	-
Equalizing Filter Spacing	-
Total Jitter pk-pk @10G	10 ps (typical)
Total Jitter pk-pk @25G	12 ps (typical)
Rise/Fall Time (20-80%) @25G	< 14 ps**
Sinusoidal Phase Modulation	30 ps
Sinusoidal Jitter Frequency	0.1 to 80 MHz
Random Jitter in Phase Modulation	30 ps (composite)
Output Return Loss up to 10GHz	<-12 dB
Output Return Loss (16-25GHz)	<-8 dB

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Advance Product information subject to change. Multilane SAL reserves the right to make changes to its product specifications at any time without notice. The information furnished herein is believed to be accurate; however, no responsibility is assumed for its use.



TX Skew Control Range	100 ps	Reference Clock Output Amplitude	550-850 mVpp
Lane to Lane Skew Resolution	0.5 ps	Reference Clock Input	Rate/32 for 8.5-15G and Rate/80 for 30G
Error Detector Phase Margin	5 ps	Reference Clock Input Amplitude	300-1900 mVpp
Error Detector Input Amplitude	110-1050 mVpp @11G, 1200 mVpp @25G	Clock Data Recovery	Rate/N (user selectable from 8 and 16)
Error Detector Maximum Input	1200 mV Diff	TX/RX and Clock Connectors in ATE	SMPM-RA
Error Detector Input Sensitivity	30 mVpp @ 10.3125G / 50 mVpp @ 28G	Power Requirement	1.9A @12 V
Phase Scan Resolution	7 bits		
Vertical Scan Resolution	8 bits		
Input CTLE Dynamic Range	10 dB		
Reference Clock Output	Rate/32 for 8.5-15G and Rate/80 for 21-30G		

*Output amplitude setting error: $\pm 50 \text{ mV} \pm 17\%$ of setting amplitude **Test condition is differential, PRBS7, 70GHz-bandwidth sampling scope with a 80cm phase-matched K(2.92mm) cable pair.

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